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Título: Layout Techniques For Mosfets

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Precio: \$875.00

Editorial:

Año: 2016

Tema:

Edición: 1ª

Sinopsis

ISBN: 9781627054881

This book aims at describing in detail the different layout techniques for remarkably boosting the electrical performance and the ionizing radiation tolerance of planar Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFETs) without adding any costs to the current planar Complementary MOS (CMOS) integrated circuits (ICs) manufacturing processes. These innovative layout styles are based on pn junctions engineering between the drain/source and channel regions or simply MOSFET gate layout change. These interesting layout structures are capable of incorporating new effects in the MOSFET structures, such as the Longitudinal Corner Effect (LCE), the Parallel connection of MOSFETs with Different Channel Lengths Effect (PAMDLE), the Deactivation of the Parallel MOSFETs in the Bird's Beak Regions (DEPAMBBRE), and the Drain Leakage Current Reduction Effect (DLECRE), which are still seldom explored by the semiconductor and CMOS ICs industries. Several three-dimensional (3D) numerical simulations and experimental works are referenced in this book to show how these layout techniques can help the designers to reach the analog and digital CMOS ICs specifications with no additional cost. Furthermore, the electrical performance and ionizing radiation robustness of the analog and digital CMOS ICs can significantly be increased by using this gate layout approach