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Título: Embedded System Design: Modeling, Synthesis And Verification

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Sinopsis

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Offers numerous practical examples for professionals

Includes case examples on industrial strength and practical standards

Covers the state-of-the-art verification methods and emerging verification techniques for system level design

Provides detailed descriptions of design techniques for various embedded software and hardware components

Describes system design flows and design methodology from system specification to prototyping

Embedded System Design: Modeling, Synthesis and Verification introduces a model-based approach to system level design. It presents modeling techniques for both computation and communication at different levels of abstraction, such as specification, transaction level and cycle-accurate level. It discusses synthesis methods for system level architectures, embedded software and hardware components. Using these methods, designers can develop applications with high level models, which are automatically translatable to low level implementations. This book, furthermore, describes simulation-based and formal verification methods that are essential for achieving design confidence. The book concludes with an overview of existing tools along with a design case study outlining the practice of embedded system design. Specifically, this book addresses the following topics in detail:

- . System modeling at different abstraction levels
- . Model-based system design
- . Hardware/Software codesign
- . Software and Hardware component synthesis

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. System verification

This book is for groups within the embedded system community: students in courses on embedded systems, embedded application developers, system designers and managers, CAD tool developers, design automation, and system engineering.